REMARKS

Applicant respectfully requests reconsideration of this application. In the Office Action, claims 19-23, 93-105, and 107-118 were pending. No claim has been amended. New claim 121-123, depending from claim 19, have been added. No new matter has been added.

Rejections under 35 U.S.C. § 102

Claims 19-23, 93-105, and 109-120 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,115,812 of Abdallah *et al.* (hereinafter "Abdallah").

Claim 19, as presented, recites:

> 19. A method comprising:
> storing **only** a plurality of non-contiguous groups of source bits into a plurality of non-contiguous groups of destination storage locations in response to execution of a first instruction that does not specify an order in which the plurality of non-contiguous groups of source bits are to be stored into the plurality of non-contiguous groups of destination storage locations; and
> **duplicating bits from the plurality of non-contiguous groups of destination storage locations** into groups of destination storage locations adjacent to the non-contiguous groups of destination storage locations. (Emphasis added)

Claim 19 requires "storing only a plurality of non-contiguous groups of source bits into a plurality of non-contiguous groups of destination storage locations in response to execution of a first instruction that does not specify an order in which the plurality of non-contiguous groups of source bits are to be stored into the plurality of non-contiguous groups of destination storage locations" and "duplicating bits from the plurality of non-contiguous groups of destination storage locations into groups of destination storage

locations adjacent to the non-contiguous groups of destination storage locations". Applicant respectfully asserts that Abdallah fails to disclose at least these limitations.

Referring to Abdallah (col. 6, line 44-55), the SHUFPS instruction, as disclosed, moves source data having data items A, B, C, and D into a destination register, with possibilities to occupy any location of a result data item (col.6, line 49-50). First of all, Abdallah merely moves source data into a destination register and does not then duplicate the data moved into the contiguous locations, as required in claim 19. There is also no mention of "duplicating bits from the plurality of non-contiguous groups of destination storage locations into groups of destination storage locations adjacent to the non-contiguous groups of destination storage locations" in Abdallah.

Claim 19 requires "storing only a plurality of non-contiguous groups of source bits into a plurality of non-contiguous groups of destination storage locations" (emphasis added). Abdallah discloses moving data elements from operand 350 ("ABCD") to an example of result data item 354 "ABDC" (Abdallah, col. 6, line 53-55). Data elements "A" and "B" are contiguous to each other (Abdallah, Figure 3E). Therefore, Abdallah fails to disclose "storing only a plurality of non-contiguous groups of source bits into a plurality of non-contiguous groups of destination storage locations" as required in claim 19.

Moreover, the SHUFPS instruction of Abdallah requires one operand (provided by the programmer) to designate the order of data items (A, B, C, and D) when stored in the destination register. When writing program, programmers provide sufficient operands in a computer instruction for a computer to operate on. In this case, the SHUFPS instruction receives at least one code indicating an operand to designate the locations for each data items to be shuffled into. Hence, Abdallah fails to disclose "a first instruction

that does not specify an order in which the plurality of non-contiguous groups of source bits are to be stored into the plurality of non-contiguous groups of destination storage locations".

For at least the foregoing reason, it is respectfully submitted that claim 19 is not anticipated by Abdallah. Claims 20-23 depend from claim 19. Applicant submits that the claims are also not anticipated by Abdallah. Accordingly, Applicant respectfully requests the rejections of claims 19-23 under 35 U.S.C. §102(b) be withdrawn.

Claims 93-100, 101-105, and 109 are rejected under 35 U.S.C. §102(b) as being anticipated by Abdallah.

Claim 93, as presented, requires "a second storage area to store only the plurality of non-contiguous groups of source bits into a plurality of non-contiguous groups of destination storage locations" (emphasis added). Claim 101, as presented, requires "the processor to store only a plurality of non-contiguous groups of source bits into a plurality of non-contiguous groups of destination storage locations" (emphasis added). As explained above with respect to claim 19, Abdallah discloses moving data elements from operand 350 ("ABCD") to an example of result data item 354 "ABDC" (Abdallah, col. 6, line 53-55). Data elements "A" and "B" are contiguous to each other (Abdallah, Figure 3E). Hence, Abdallah fails to teach "store only a plurality of non-contiguous groups of source bits into a plurality of non-contiguous groups of destination storage locations" as required by the claims.

For at least the foregoing reason, Applicant submits that claims 93 and 101 are not anticipated by Abdallah. Claims 94-100, 102-105, and 109 depend from one of the above independent claims. It is respectfully submitted that the claims are therefore not

anticipated by Abdallah. Accordingly, Applicant respectfully requests the rejections of claims 93-100, 101-105, and 109 under 35 U.S.C. §102(b) be withdrawn.

Claims 110-120 are rejected under 35 U.S.C. 102(b) as being anticipated by Abdallah.

Claim 110, as presented, recites:

> 110. A machine-readable medium having stored thereon an instruction, which if executed by a machine, causes the machine to perform a method comprising:
> storing bits [31-0] of a source value into bit storage locations [63-32] and [31-0] of a destination register;
> storing bits [95-64] of the source value into bit storage locations [127-96] and [95-64] of the destination register, **wherein the instruction does not include a code to designate the order in which the source bits are to be stored in the destination register**. (Emphasis added)

Applicant respectfully asserts that Abdallah fails to disclose at least "wherein the instruction does not include a code to designate the order in which the source bits are to be stored in the destination register" as required by claim 110. As explained in the Office Action, Abdallah mentions that the operand source bits are copied to any location of the result. The Office Action agrees that Abdallah is silent about whether "an order must be directly specified in the instruction". The SHUFPS instruction of Abdallah requires one operand (provided by the programmer) to designate the order of data items (A, B, C, and D) when stored in the destination register. In this case, the SHUFPS instruction receives at least one code indicating an operand to designate the locations for each data items to be shuffled into. Result 354 remains unknown unless at least one operand (provided by the programmer) is used to designate the order of data items (A, B, C, and D) when stored in the destination register. Therefore, Abdallah fails to disclose at least "wherein the

instruction does not include a code to designate the order in which the source bits are to be stored in the destination register" as required in claim 110. Applicant would like to assert that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.

For at least the foregoing reasons, Applicant believes that claim 110 is allowable over Abdallah. Applicant respectfully requests the withdrawal of the rejection for the claim 110. Moreover, dependent claims 111 and 112 depend from independent claim 110. Applicant believes that claim 110 is allowable such that claims 111 and 112 depending therefrom with additional limitations are also allowable. Applicant respectfully requests the rejections of claims 110-112 under 35 U.S.C. §102(b) be withdrawn.

Similarly, independent claims 113, 116, 119-120 were rejected using a similar example in the Office Action. The detailed remarks with respect to independent claim 110 are incorporated here by reference. Moreover, claims 119-120 further requires "duplicating bits from the bit storage" which Abdallah fails to disclose as explained above with respect to claim 19. The remarks are incorporated herein by reference.

For the reasons similar to those discussed above, it is respectfully submitted that claims 113, 116, and 119-120 are not anticipated by Abdallah. Claims 114 and 115 depend from independent claims 113. Claims 117 and 118 depend from independent claim 116. Hence, it is respectfully submitted that the claims 113-120 are not anticipated by Abdallah. Accordingly, Applicant respectfully requests the rejections of the claims under 35 U.S.C. §102(b) be withdrawn.

Rejections under 35 U.S.C. § 103

Claims 107 and 108 are rejected under 35 U.S.C. §103(a) as being obvious over Abdallah.

Claims 107 and 108 depending indirectly on independent claim 101, are rejected under 35 U.S.C. 103(a) as being unpatentable over Abdallah. As presented above in traversing the 35 U.S.C rejections of the independent claim 101, Abdallah fails to teach every limitation of independent claim 101. No other reference was cited by the Examiner to cure those deficiencies of Abdallah. Thus, claims 107 and 108, which depend from the above independent claim, are patentable over Abdallah. Accordingly, Applicant respectfully requests that the 35 U.S.C. §103(a) rejection of claims be withdrawn.

New Claims

Applicant has presented three new dependent claims. Claim 121-123 depends from claim 19. In view of the foregoing reasons, independent claims 19 is allowable and therefore the dependent claims 121-123 are also allowable over the cited reference.

Claim 121 requires "wherein the order in which the non-contiguous groups of source bits are to be stored into the non-contiguous groups of destination storage locations is fixed". Claim 122 requires "wherein the order in which the non-contiguous groups of source bits are to be stored into the non-contiguous groups of destination storage locations is specific in accordance with the first instruction". Claim 123 requires "wherein the first instruction is associated with one unique order of in which the non-contiguous groups of source bits are to be stored into the non-contiguous groups of destination storage locations". The cited reference fails to teach the limitations as set forth in the claims above.

Therefore, at least for the foregoing reasons, Applicant submits that claims 121-123 are allowable. Applicant respectfully requests the allowance for claims 121-123.

CONCLUSION

Applicant respectfully submits that the rejections have been overcome by the remarks, and that the pending claims are in condition for allowance. Accordingly, Applicant respectfully requests the rejections be withdrawn and the pending claims be allowed.

Pursuant to 37 C.F.R. §1.136(a)(3), Applicant hereby requests and authorizes the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,
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